IEEE 1149.4 JTAG
Analog Test Access Port and Standard
Topics to be Covered

- Motivation
- Bus overview
- Hardware faults
- Test Bus Interface Circuit (TBIC)
- Analog Boundary Module (ABM)
- Instructions
- Specialized Bus Circuits
- Summary
Purpose of Analog JTAG Standard

- For a System-on-a-Chip (SOC):
  - Cannot assume that we are interconnecting pre-tested modules
  - Internal module probing is impractical
  - Solution: Use boundary scan structure to partition analog, digital, and memory sub-systems in SOC and test each separately

- Analog JTAG test capability:
  - Oriented towards measuring external component values or internal impedances (shorts, opens, wrong components)
  - Not intended for DSP type analog tests
Analog Test Bus

- **PROs:**
  - Usable with digital JTAG boundary scan
  - Adds analog testability – both controllability and observability
  - Eliminates large area needed for analog test points

- **CONs:**
  - May have a 5% measurement error
  - C-switch sampling devices couple all probe points capacitively, even with test bus off – requires more elaborate (larger) switches
  - Stringent limit on how far data can move through the bus before it must be digitized to retain accuracy
Analog Test Bus Diagram

Digital I/O

Mixed-signal circuitry

ATAP

Test bus interface circuit

AB1

AB2

Control signals

Test control block

TAP

Test Access Port

Analog Test Access Port

TCB -- 1149.1 TAP, Instruction reg., & decode

April 24, 2006
Analog Boundary Module

From TDI-TDO chain

From analog circuit

1-bit digitizer

Uncommitted, usable for ABM test

To TDI-TDO chain

From TAP controller

Control decode logic

M1  M2

D

C  U

B1

C  U

B2

C  U

SL

SG

SB1

SB2

SH

SD

V_H

V_L

V_G

V_TH

SL

SH

SB1

SB2

Analog pin

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Analog Defects and Faults

- Extended Interconnect
- Short

- Misloaded Device

- Open

- Wrong Value

- Simple Interconnect
- Short

- Differential Interconnect
  (Analog or Digital)

- Single-Ended Transmission Point

- Single-Ended Reception Point
Need for Discrete Components

- Impedance matching of transmission lines necessary – merchant ICs will not have built-in impedance matching resistances
- Discrete resistors use much power – may prevent them from being on-chip
- Impossible to make high-valued, accurate inductors or transformers on chip
- Integrated R, C, L components are never as precise as external ones
- Some ICs can be extended to more functions if external R, C, or L value can be changed
Measurement Limitations with 1149.4

- Must test device with power on
- Multiplexing done with silicon devices, not relays
- Introduces unwanted impedances during testing
- Has additional current leakages to ground
- CMOS silicon switches non-linear over larger signal swings – may also be slow
- 1149.4 bus has less than 1 MHz bandwidth
## Switch Limitations

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Relay</th>
<th>CMOS</th>
<th>Bipolar</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-resistance</td>
<td>$10^{-2}$ W</td>
<td>$10^2$ to $10^3$ W</td>
<td>Varies</td>
</tr>
<tr>
<td>Off-resistance</td>
<td>$10^{12}$ W</td>
<td>$10^{12}$ W</td>
<td>$10^{10}$ W</td>
</tr>
<tr>
<td>Bidirectional?</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Switching time</td>
<td>$\geq 500$ ms</td>
<td>$&lt; 1$ ms</td>
<td>$&lt; 1$ ms</td>
</tr>
<tr>
<td>Area $\text{mm}^2$</td>
<td>$96.7 \times 10^6$</td>
<td>20</td>
<td>100 to 5000</td>
</tr>
</tbody>
</table>
Chaining of 1149.4 ICs
Analog Test Access Port

- TDI, TDO, TCK, TMS signals from Digital standard are required
- TRST signal from Digital standard is optional
- New required analog signals:
  - AT1 – for analog stimulus
  - AT2 – for sending analog response to ATE
  - AT1 and AT2 can be partitioned
- Digital part same as before, except:
  - New Test Bus Interface Circuit (TBIC)
  - Multiple digital pin cells grouped into Digital Boundary Module (DBM)
  - Set of cells required to control analog pin grouped into Analog Boundary Module (ABM)
Test Bus Interface Circuit

For Interconnect Test Logic Value Selection

For Isolation and Characterization Bus-to-Bus Switching
TBIC Functions

- Connect or isolate analog measurement buses $AB1$ and $AB2$ within chip to or from external $AT1$ and $AT2$ signals
- Perform 1149.1 interconnect tests on $AT1$ and $AT2$ pins
  - Support coarse digitization relative to threshold $V_{TH}$
- Support analog characterization measurements
  - Clamp busses not being driven
# TBIC Switching Patterns

<table>
<thead>
<tr>
<th>Switch state S1-S10 for patterns given in book</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>$AT_n$ disconnect (high Z), clamp $AB_n$</td>
</tr>
<tr>
<td>1</td>
<td>Connect $AT_2$ &amp; $AB_2$</td>
</tr>
<tr>
<td>2</td>
<td>Connect $AT_1$ &amp; $AB_1$</td>
</tr>
<tr>
<td>3</td>
<td>Connect $AT_n$ &amp; $AB_n$</td>
</tr>
<tr>
<td>4</td>
<td>$AT_1/2$ drive 00 out</td>
</tr>
<tr>
<td>5</td>
<td>$AT_1/2$ drive 01 out</td>
</tr>
<tr>
<td>6</td>
<td>$AT_1/2$ drive 10 out</td>
</tr>
<tr>
<td>7</td>
<td>$AT_1/2$ drive 11 out</td>
</tr>
<tr>
<td>8</td>
<td>For characterization</td>
</tr>
<tr>
<td>9</td>
<td>For characterization</td>
</tr>
</tbody>
</table>

For characterization

For characterization

$P_1 - P_3$ for analog measurement

$P_0$ & $P_4$ -- $P_7$ for 1149.1 interconnect test
TBIC Switch Controls

Towards TDO

From TAP Controller

Mode2

Mode1

From TBIC Digitizers

DAT2

DAT1

CU

CU

CU

Uncommitted, may be used for improved TBIC testability

From TDI

TBC Control Decode Logic

M1

M2

D1

D2

Co

Ca

S1

S2

S3

S4

S5

S6

S7

S8

S9

S10

C -- Master-Slave Flip-Flop

U -- Hold latch to prevent shifting from disturbing the TBIC state

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Analog Boundary Module Has Four Control Cells

- Work in conjunction with TBIC and various 1149.4 bus modes to set state for one analog pin:
  - Calibrate (Ca)
  - Control (Co)
  - Data1 (D1)
  - Data2 (D2)
- Test mode determined by 4 ABM digital pins and by TBIC switches $S1-S10$
# ABM Switch Patterns

<table>
<thead>
<tr>
<th>Pattern #</th>
<th>Pin State</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Completely isolated</td>
</tr>
<tr>
<td>1</td>
<td>Monitored (mon.) by AB2</td>
</tr>
<tr>
<td>2</td>
<td>Connected (conn.) to AB1</td>
</tr>
<tr>
<td>3</td>
<td>Conn. to AB1, mon. by AB2</td>
</tr>
<tr>
<td>4</td>
<td>Connected to VG</td>
</tr>
<tr>
<td>5</td>
<td>Conn. to VG, mon. by AB2</td>
</tr>
<tr>
<td>6</td>
<td>Conn. to VG &amp; AB1</td>
</tr>
<tr>
<td>7</td>
<td>Conn. to VTG &amp; AB1, mon. by AB2</td>
</tr>
<tr>
<td>8</td>
<td>Conn. to VL</td>
</tr>
<tr>
<td>9</td>
<td>Conn. to VL, mon. by AB2</td>
</tr>
<tr>
<td>10</td>
<td>Conn. to VL &amp; AB1</td>
</tr>
<tr>
<td>11</td>
<td>Conn. to VL &amp; AB1, mon. by AB2</td>
</tr>
<tr>
<td>12</td>
<td>Conn. to VH</td>
</tr>
<tr>
<td>13</td>
<td>Conn. to VH, mon. by AB2</td>
</tr>
<tr>
<td>14</td>
<td>Conn. to VH &amp; AB1</td>
</tr>
<tr>
<td>15</td>
<td>Conn. to VH &amp; AB1, mon. by AB2</td>
</tr>
<tr>
<td>16</td>
<td>Conn. to core, isolated from test</td>
</tr>
<tr>
<td>17</td>
<td>Conn. to core, mon. by AB2</td>
</tr>
<tr>
<td>18</td>
<td>Conn. to core &amp; AB1</td>
</tr>
<tr>
<td>19</td>
<td>Conn. to core &amp; AB1, mon. by AB2</td>
</tr>
</tbody>
</table>

**SD, SH, SL, SG, SB1, SB2**

Switch states for the pattern given in book

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# TBIC Patterns & ABM Values

<table>
<thead>
<tr>
<th>4 Cells</th>
<th>EXTEST</th>
<th>PROBE</th>
<th>HIGHZ</th>
<th>BYPASS, SAMPLE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>CLAMP</td>
<td>INTEST</td>
<td></td>
<td>PRELOAD, IDC</td>
</tr>
<tr>
<td></td>
<td>RUNBIST</td>
<td></td>
<td>USERCODE</td>
<td>CODE USERCODE</td>
</tr>
<tr>
<td>0000</td>
<td>P0</td>
<td>P0</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>0001</td>
<td>P1</td>
<td>P1</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>0010</td>
<td>P2</td>
<td>P2</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>0011</td>
<td>P3</td>
<td>P3</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>0100</td>
<td>P4</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>0101</td>
<td>P5</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>0110</td>
<td>P6</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>0111</td>
<td>P7</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1000</td>
<td>P0</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1001</td>
<td>P8</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1010</td>
<td>P9</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1011</td>
<td>*</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1100</td>
<td>*</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1101</td>
<td>*</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1110</td>
<td>*</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
<tr>
<td>1111</td>
<td>*</td>
<td>*</td>
<td>P0</td>
<td>P0</td>
</tr>
</tbody>
</table>
Analog Boundary Module Functions

- One-bit digitizer captures pin voltage and interprets it as digital
- Simultaneously provides one more of these functions at an analog pin:
  - Connect pin to $V_L$
  - Connect pin to $V_H$
  - Connect pin to $V_G$ (reference quality)
  - Connect pin to $AB1$ (provides current)
  - Connect pin to $AB2$ (monitors voltage)
Electro-Static Discharge Protection for ABM

(a) Ordinary pin

(b) ABM pin
EXTEST Instruction

- Can disable or enable each of these connections for each analog pin:
  - *Core-disconnect state* (disconnected from internal analog circuitry)
  - Connect to $V_L$
  - Connect to $V_H$

- Had to be individually pin programmable, because bias voltage pins can never be disconnected, and low impedance $R$’s or $L$’s often cannot be disconnected

- *Core-disconnect state* often not implemented with a transistor, since that can reduce driver performance
ATE External Impedance Measurement with EXTEST

![Diagram of ATE System with Test Controller, Power Supply, Digital Test Sequencer, and IC labeled 1149.4 with terminals 1 and 2, input signals TDI, TCK, TMS, voltage input V, and current input i, and output signals AT1, AT2, and TDO.]
1149.4 Measurement of External Impedance

(a) Pin 1 voltage measurement
Pin 2 Voltage Measurement

$$Z = \frac{V_{Pin1} - V_{Pin2}}{I}$$
CLAMP and HIGHZ Instructions

- **CLAMP** – Disconnects all pins from cores and freezes analog pins in present state
  - Freezes TBIC in present state
  - Keeps circuit quiescent, while $V$ and $I$ are measured in other parts
- **HIGHZ** – Opens core disconnect switch $SB$
  - Disconnects all test circuits
  - Disables TBIC
New PROBE Instruction

- Required
- Works similarly to digital SAMPLE instruction
- Operates on both digital and analog pins
- Allows continuous time sampling while analog core is functioning
  - Can only sample 1 analog pin at a time (only 1 set of ABn wires exists)
  - Sets all Analog and Digital Boundary Modules to connect all pins to cores
- AB switch may add parasitic element into circuit
- Most useful for noise measurements
- Can make f measurements only up to 1 kHz
At any time, only 1 analog pin can be stimulated and only 1 analog pin can be read.
RUNBIST and SAMPLE / PRELOAD Instructions

- **RUNBIST** – operates exactly as in 1149.1 digital standard
  - Analog pins can either mimic **HIGHZ** or **CLAMP** instructions
- **SAMPLE / PRELOAD** – for Analog pins
  - Digitizes the analog pin voltage
    - Stored as ‘1’ if > $V_{TH}$, otherwise as ‘0’
    - Stored in boundary register
Differential Interconnect

- Greatly improves common-mode noise rejection
  - Can still work, even when single lines or $R$’s are opened or shorted

![Diagram of differential interconnect system](image-url)
Partitioned AB Busses
Isolation of Analog and Digital Cores

- 1149.4 standard requires that a digital boundary module be on each digital line between digital and analog core
  - Only when \textit{INTEST} or \textit{RUNBIST} instructions supported, otherwise can eliminate DBM
- Can use analog boundary module to test digital pins & interconnect with 1149.4
Analog Switch to Reduce Coupling
Guarding Between Signals

(a) Pin guard.  (b) Guard wire.  (c) Driven guard.
Summary

- Analog test bus allows static analog tests
- Non-static or feedback circuits are hard to test
- Good for locating shorts, opens, and wrong external component values
  - $V_H$ and $V_L$ switches in ABM must be able to survive large voltage differences
- Needs customizing digitizing receiver for digitizing analog bus – inverter not suitable
- Can eliminate separate process monitor transistors and resistors on wafers – saves area
- Needs large, low-resistance transistor switches to avoid common mode measurement errors