$I_{DDQ}$ Current Testing
Motivation

- Early 1990’s – Fabrication Line had 50 to 1000 defects per million (dpm) chips
  - IBM wanted to get 3.4 defects per million (dpm) chips
- Conventional way to reduce defects:
  - Increasing test fault coverage
  - Increasing burn-in coverage
  - Increase Electro-Static Damage awareness
- New way to reduce defects:
  - $I_{DDQ}$ Testing
    - Also useful for Failure Effect Analysis
Basic Principle of $I_{DDQ}$ Testing

- Measure $I_{DDQ}$ current through $V_{SS}$ bus
Faults Detected by $I_{DDQ}$ Tests
Stuck-at Faults Detected by $I_{DDQ}$ Tests

- **Bridging faults** with stuck-at fault behavior
  - Bridging of a logic node to $V_{DD}$ or $V_{SS}$
    - These are a small percentage of the real defects.
  - *Transistor gate oxide short* of 1 KΩ to 5 KΩ to source.
    - Also causes a stuck-at fault.

- Floating MOSFET gate defects
  - Elevates $I_{DDQ}$ currents.
  - Do not fully turn off transistor.
NAND Open Circuit Defect – Floating gate
Floating Gate Defects

- Small break in logic gate inputs (100 – 200 Angstroms) lets wires couple by electron tunneling.
  - Causes both delay fault and $I_{DDQ}$ fault.
- Large open results in stuck-at fault – not detectable by $I_{DDQ}$ test.
  - If $V_{tn} < V_{fn} < V_{DD} - |V_{tp}|$ then detectable by $I_{DDQ}$ test
Multiple $I_{DDQ}$ Fault Example
Capacitive Coupling of Floating Gates

- $C_{pb}$ – capacitance from poly to bulk
- $C_{mp}$ – overlapped metal wire to poly
- Floating gate voltage depends on capacitances and node voltages
- If $n$-FET and $p$-FET get enough gate voltage to turn them on, then $I_{DDQ}$ test detects this defect
- $K$ is the transistor gain
$I_{DDQ}$ Current Transfer Characteristic

Segura et al. – 5 defective inverter chains (1-5) with floating gate defects
Bridging Faults $S_1 - S_5$

- Caused by absolute short ($< 50 \, \Omega$) or higher $R$
- Segura et al. evaluated testing of bridges with 3 CMOS inverter chain
- $I_{DDQ_{R_b}}$ tests fault when $R_b > 50 \, \text{K}\Omega$ or $0 \leq R_b \leq 100 \, \text{K}\Omega$
- Largest deviation when $V_{in} = 5 \, \text{V}$ bridged nodes at opposite logic values
$S1 \ I_{DDQ}$ Depends on $K, R_b$

![Graph showing the relationship between $K$, $R_b$, and $I_{DDQ}$](image-url)
CMOS Transistor Stuck-Open Faults

- CMOS transistor stuck-open faults cause high impedance states at a logic gate output.
  - $I_{DDQ}$ test can sometimes detect fault.
  - Works in practice due to body effect.
- $IDDQ$ testing does not guarantee detection, but works in practice because the floating output node is capacitively coupled to the substrate, as well.
Delay Faults

- Most random CMOS defects cause a timing delay fault, rather than a catastrophic failure.
- Many delay faults detected by $I_{DDQ}$ test.
  - Many delay faults detected with few $I_{DDQ}$ test vectors.
  - Late switching of logic gates keeps $I_{DDQ}$ elevated.
- Some delay faults are not detected by $I_{DDQ}$ test.
  - Resistive via fault in interconnect.
  - Increased transistor threshold voltage fault.
Leakage Faults

- Gate oxide shorts cause leaks between gate & source, or gate & drain.
- Mao and Gulati leakage fault model:
  - Leakage path faults: $f_{GS}$, $f_{GD}$, $f_{SD}$, $f_{BS}$, $f_{BD}$, $f_{BG}$
    - $G$ = gate, $S$ = source, $D$ = drain, $B$ = bulk
- Assume that short does not change logic values.
  - These shorts may later develop into hard faults, which cause field failures.
Weak Faults

- $n$FET passes logic 1 as $5 \text{ V} - V_{tn}$
- $p$FET passes logic 0 as $0 \text{ V} + |V_{tp}|$
- *Weak fault* – one device in C-switch does not turn on
  - Causes logic value degradation in C-switch
Paths in Circuit

- Normal 1 conducting path $V_{DD}$ to $O1$
- Weak 1 conducting path $V_{DD}$ to $O1$
- Normal 1 transmission path $V_{SS}$ to $A$

$I_1$, $I_2$, $P_1$, $P_2$, $P_3$, $P_4$, $P_5$, $P_6$, $N_1$, $N_2$, $N_3$, $N_4$, $N_5$, $N_6$, $O_1$, $O_2$
Transistor Stuck-Closed Faults

- Due to *gate oxide short* (GOS)
- \( k = \text{distance of short from drain} \)
- \( R_s = \text{short resistance} \)
- \( I_{DDQ2} \) current results show 3 or 4 orders of magnitude elevation
Gate Oxide Short
Logic and $I_{DDQ}$ Testing Zones
$I_{DDQ}$ Testing Methods
Fault Coverage Metrics

- **Conductance fault model** (Malaiya & Su)
  - Monitor $I_{DDQ}$ to detect all leakage faults
  - Proved that stuck fault test set can be used to generate minimum leakage fault test set

- **Short fault coverage**
  - Handles intra-gate bridges, but may not handle inter-gate bridges

- **Pseudo-stuck-at fault coverage**
  - Voltage stuck-at fault coverage that represents internal transistor short fault coverage and hard stuck-at fault coverage
Fault Coverages for $I_{DDQ}$ Fault Models
Vector Selection with Full Scan

- Use voltage testing & full scan for $I_{DDQ}$ tests
- Measure $I_{DDQ}$ current when voltage vector set hits internal scan boundary
  - Set all nodes, inputs & outputs in known state
  - Stop clock & apply minimum $I_{DDQ}$ current vector
  - Wait 30 ms for settling, measure $I_{DDQ}$ against 75 µA Limit, with 1 µA accuracy
QUIETEST Leakage Fault Detection

- Sensitize *leakage fault*.
- Detection – 2 transistor terminals with leakage must have opposite logic values, and be at driving strengths.
- Non-driving, high-impedance states won’t work – current cannot go through them.
Weak Fault Detection – P1 (N1) Open

- Elevates $I_{DDQ}$ from 0 $\mu$A to 56 $\mu$A
Second Weak Fault Detection Example

- Not detected unless $I_3 = 1$
Hierarchical Test Vector Selection

- Generate complete stuck-fault tests.
- Characterize each logic component – relate input/output logic values & internal states:
  - To leakage fault detection
  - To weak fault sensitization/propagation
  - Uses switch-level simulation (done only once for each component type to characterize it).
- Store this information in leakage & weak fault tables.
- Logic simulate stuck-fault tests – use tables to find faults detected by each vector.
  - No more switch-level simulation
Leakage Fault Table

- \( k = \# \) component I/O pins
- \( n = \# \) component transistors
- \( m = 2^k \) (# of input / output combinations)
- \( m \times n \) matrix \( M \) represents the table
- Each logic state – 1 matrix row
- Entry \( m_{ij} = \) octal leakage fault information
  - Flags \( f_{BG} f_{BD} f_{BS} f_{SD} f_{GD} f_{GS} \)
  - Sub-entry \( m_{ij} = 1 \) if leakage fault detected
Example Leakage Fault Table

(a) Logic circuit.  (b) Logic simulation.  (c) Leakage fault table.
Weak Fault Table

- Weak faults:
  - Sensitized by input/output states of faulty component
  - Propagated by either faulty component input/output states or input/output states of components driven by node with weak fault
- Use weak fault detection, sensitization, and propagation tables
**$I_{DDQ}$ Test Vector Selection**

- If vector tests one new leakage/weak fault, select it for $I_{DDQ}$ measurement
- Example circuit:
## Results – Logic & $I_{DDQ}$ Tests

<table>
<thead>
<tr>
<th>Time</th>
<th>$I1$</th>
<th>$I2$</th>
<th>$X1$</th>
<th>$O1$</th>
<th>Time</th>
<th>$I1$</th>
<th>$I2$</th>
<th>$X1$</th>
<th>$O1$</th>
</tr>
</thead>
<tbody>
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<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

$I_{DDQ}$ measurement vectors in green

Time in units
## QUIETEST Results

<table>
<thead>
<tr>
<th>Ckt.</th>
<th># of Transistors</th>
<th># of Leakage Faults</th>
<th>% Selected Vectors</th>
<th>Leakage Fault Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>7584</td>
<td>39295</td>
<td>0.5 %</td>
<td>94.84 %</td>
</tr>
<tr>
<td>2</td>
<td>42373</td>
<td>220571</td>
<td>0.99 %</td>
<td>90.50 %</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Ckt.</th>
<th># of Weak Faults</th>
<th>% Selected Vectors</th>
<th>Weak Fault Coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1923</td>
<td>0.35 %</td>
<td>85.3 %</td>
</tr>
<tr>
<td>2</td>
<td>1497</td>
<td>0.21 %</td>
<td>87.64 %</td>
</tr>
</tbody>
</table>
Instrumentation Problems

- Need to measure < 1 µA current at clock > 10 kHz.
- Off-chip $I_{DDQ}$ measurements degraded
  - Pulse width of CMOS IC transient current
  - Impedance loading of tester probe
  - Current leakages in tester
  - High noise of tester load board
- Much slower rate of current measurement than voltage measurement.
IBM Graphics controller chip – CMOS ASIC, 166,000 standard cells
0.8 µm static CMOS, 0.45 µm Lines ($L_{\text{eff}}$), 40 to 50 MHz Clock, 3 metal layers, 2 clocks
Full boundary scan on chip
Tests:
- Scan flush – 25 ns latch-to-latch delay test
- 99.7% scan-based stuck-at faults (slow 400 ns rate)
- 52% SAF coverage functional tests (manually created)
- 90% transition delay fault coverage tests
- 96% pseudo-stuck-at fault cov. $I_{\text{DDQ}}$ Tests
**SEMATECH Results**

- Test process: Wafer Test → Package Test → Burn-In & Retest → Characterize & Failure Analysis
- Data for devices failing some, but not all, tests.

<table>
<thead>
<tr>
<th>Scan-based Stuck-at</th>
<th>IDDQ (5 µA limit)</th>
<th>Functional</th>
</tr>
</thead>
<tbody>
<tr>
<td>pass</td>
<td>pass</td>
<td>fail</td>
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<tr>
<td>pass</td>
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<td>1463</td>
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<tr>
<td>fail</td>
<td>14</td>
<td>0</td>
</tr>
<tr>
<td>pass</td>
<td>6</td>
<td>1</td>
</tr>
<tr>
<td>fail</td>
<td>52</td>
<td>36</td>
</tr>
<tr>
<td>pass</td>
<td>fail</td>
<td>pass</td>
</tr>
</tbody>
</table>
Hard to find point differentiating good and bad devices for $I_{DDQ}$ & delay tests

High # passed functional test, failed all others

High # passed all tests, failed $I_{DDQ} > 5 \mu A$

Large # passed stuck-at and functional tests
  - Failed delay & IDDQ tests

Large # failed stuck-at & delay tests
  - Passed $I_{DDQ}$ & functional tests

Delay test caught delays in chips at higher Temperature burn-in – chips passed at lower T.
Limitations of $I_{DDQ}$ Testing

- Sub-micron technologies have increased leakage currents.
  - Transistor sub-threshold conduction.
  - Harder to find $I_{DDQ}$ threshold separating good & bad chips.

- $I_{DDQ}$ tests work:
  1. When average defect-induced current is greater than average good IC current.
  2. Small variation in $I_{DDQ}$ over test sequence & between chips.

- Now less likely to obtain the above two conditions.
Summary

- $I_{DDQ}$ tests improve reliability, find defects causing:
  - Delay, bridging, weak faults
  - Chips damaged by electro-static discharge
- No natural breakpoint for current threshold.
  - Get continuous distribution – bimodal would be better
- Conclusion: now need stuck-fault, $I_{DDQ}$, and delay fault testing combined.
- Still uncertain whether $I_{DDQ}$ tests will remain useful as chip feature sizes shrink further