DSP Based Analog and Mixed Signal Test
Outline

- Motivation
- Present state-of-the-art
- Advantages of DSP-based analog tester
- Components of DSP-based analog tester
- Static A/D converter test
- Static D/A converter test
- Summary
Analog and Mixed Signal Trends

- ICs with analog, digital, and mixed-signal circuits on the same substrate are now common.
  - To reduce circuit packaging and assembly costs.
  - Explosive growth in application areas.

- Typical mixed-signal hardware systems:
  - Digital cores, frequently for DSP.
  - Surrounded by analog filters, ADCs, DACs.
  - The analog portion interfaces to the real world.
Some characteristics:
- Analog transistors and components are vastly larger than digital transistors.
- Analog circuit contains fewer than 100 devices.
- Digital part can contain millions of devices.

For mixed-signal circuits:
- Testing becomes even more of a problem.
- Analog circuit signal observability is reduced in a mixed-signal system.
Present Trend

- Designers are moving from non-linear to linear analog circuits.
  - Since linear analog circuits are easier to test.
- What to do with the non-linear part then?
  - Move the non-linear signal processing into a DSP processor in the digital part of the system.
  - Advantages gained:
    - Greater accuracy.
    - Easier design and testing.
Differences from Digital Testing

- Size not a problem – at most 50 to 100 components.
- Much harder analog device modeling
  - No widely-accepted analog fault model.
  - Infinite signal range, and a range of good signal values.
  - Tolerances depend on process and measurement error.
  - Tester (ATE) introduces measurement error.
  - Digital / analog substrate (capacitive) coupling noise.
Differences (contd.)

- Absolute component tolerances \( \pm 20\% \), relative \( \pm 0.1\% \).
  - Multiple analog fault model mandatory.
  - Effects of faults can cancel each other.
  - Fault set too large to enumerate.
- No unique signal flow direction.
Differences (contd.)

- Analog sub-components cannot be individually tested as in digital circuits.
- Test busses harder to realize for analog test:
  - Transporting an analog signal to an input pin may alter the signal and circuit functionality.
  - Reconfiguring an analog circuit during test is often unacceptable – can change analog transfer function.
  - Bus not designed to test frequency response – only tests that a specific R, L, or C has the expected value.
Present-Day Analog Testing Methods

- Specification-based (functional) tests:
  - Main method for analog testing – tractable and does not need an analog fault model.
  - Intractable for digital -- # tests is huge.

- Structural ATPG:
  - Widely used for digital, just beginning to be used for analog.

- Separate tests for functional and timing performance not possible in analog circuits.
  - Possible in digital circuits.
DSP-Based Tester Benefits over Purely Analog Tester

- More accurate:
  - Reduces crosstalk, noise, signal drift.
  - Less non-linearity.
  - Component aging less troublesome.
  - Thermal effects less troublesome.

- Faster when making multiple measurements.
- More repeatable testing.
- Easier calibration.
- Smaller, cheaper, and uses less power.
Drawbacks of DSP-based Tester

- It is expensive.
  - Desired precision may require a costly DSP.
- When making one measurement, a purely analog tester is significantly cheaper.
  - DSP-based tester is advantageous when multiple measurements are to be made.
    - Can acquire one set of samples for a DUT using one relay switching period, one sampling period, and one settling time.
    - Analysis using DFT or FFT can produce many different emulated analog test instrument measurements.
Conventional Analog Tester

- Used in 1940s onwards.
- There is no frequency-time synchronization between the stimulus generation and response analysis parts of the instrument.
  - Block diagram in next slide.
Analog Tester (Block Diagram)
DSP-Based Test System

- Replace purely analog instruments with
  - a high-speed ADC,
  - a memory for storing sample values, and
  - a DSP controlled by software routines.

- Waveform synthesizer and response analyzer are synchronized.

- Can emulate a wide variety of existing instruments.
Mixed-Signal Testing (Block Diagram)
## Time Comparison (Analog vs. DSP)

- Requires phase-lock synchronization between stimulus and sampling

<table>
<thead>
<tr>
<th>Component of 1 kHz Amplitude Measurement</th>
<th>DSP ATE</th>
<th>Analog ATE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Relay Switching</td>
<td>5 ms</td>
<td>5 ms</td>
</tr>
<tr>
<td>Load &amp; Start Synthesizer</td>
<td>5 ms</td>
<td>N/A</td>
</tr>
<tr>
<td>Synthesizer + DUT Settling</td>
<td>1 ms</td>
<td>N/A</td>
</tr>
<tr>
<td>Filter + Detector + DUT Settling</td>
<td>N/A</td>
<td>35 ms</td>
</tr>
<tr>
<td>Digitization Interval</td>
<td>1 ms</td>
<td>N/A</td>
</tr>
<tr>
<td>Transfer Time</td>
<td>1 ms</td>
<td>N/A</td>
</tr>
<tr>
<td>Computer Overhead</td>
<td>N/A</td>
<td>10 ms</td>
</tr>
<tr>
<td>DSP Processing/Overhead</td>
<td>15 ms</td>
<td>N/A</td>
</tr>
<tr>
<td>Total</td>
<td>28 ms</td>
<td>50 ms</td>
</tr>
</tbody>
</table>
DSP Tester Characteristics

- DSP-based ATE is nearly always more accurate than analog ATE.

- DSP requirement:
  - We need a very fast DSP processor.
  - Double-precision floating-point arithmetic.

- Phase-lock synchronization requirement:
  - Vector samples must fall in exactly the right places in the right time interval.
  - The digitizing window must be coordinated with each clock.
  - This is implemented with a common reference frequency, controlled by a phase-locked loop (PLL).
Waveform Synthesis

Diagram:
- Digital pattern from DSP processor
- Addressing and timing
- RAM
- D/A
- Reconstruction filter
- Analog waveform to DUT
- Phase-lock to waveform digitizer
Waveform Sampling

Sampling rate $> 100$ ks/s
ATE Clock Generator

WS = waveform source     WM = waveform measurement

Integrated clock generator in digital pattern generator
Dual analog clock to each DSP (SMS) source and measurement unit
and selected pins
set master clock \(1\) \(2\) frequency period to \(<\text{double}>\) times over \(<\text{int}>\)

connect dp master clock \(\{\)
  \{ internal reference
doubled reference
  source1
  source2
\}

to pm line \(<\text{word1}>\)

clock ws main mem with pm clock \(<\text{word1}>\)
divide by \(<\text{word2}>\)

set wm to pm clk \(<\text{word1}>\) divide by \(<\text{word2}>\)
A/D and D/A Converter Static Testing Methods
A/D and D/A Test Parameters

- A/D -- Uncertain map from input domain voltages into digital value (not so in D/A)
  - Two converters are NOT inverses
- Transmission parameters affect multi-tone tests
  - Gain, signal-to-distortion ratio, noise power ratio, differential phase shift, etc.
- Intrinsic parameters – Converter specifications
  - Full scale range (FSR), gain, # bits, static linearity (differential and integral), maximum clock rate, code format, settling time (D/A), glitch area (D/A)
Ideal Transfer Functions

A/D Converter  

D/A Converter
Offset Error

(a) ADC offset error in transfer function.

(b) DAC offset error in transfer function.
Gain Error

(a) ADC gain error in transfer function.

(b) DAC gain error in transfer function.
D/A Transfer Function Non-Linearity Error

(a) DAC irregular displacement (differential nonlinearity).

(b) DAC dependent displacement (superposition error).
Static Linearity Test

The diagram illustrates the comparison between actual and ideal digital output responses as a function of analog input. The FSR (Full Scale Range) is shown on the vertical axis, with digital outputs ranging from 000 to 110. The analog input is segmented into intervals from 0 to 3/4, and the diagram shows the step-wise deviations between actual and ideal responses at specific input values.
Differential Linearity Error

- Differential linearity function – How each code step differs from ideal or average step (by code number), as fraction of LSB.
- Subtract average count for each code tally, express that in units of LSBs.
- If DLE is less than –1, the code is declared as missing.
- Repeat test waveform 100 to 150 times, use slow triangle wave to increase resolution.
Integral Linearity Error

- The ILE is the integration of the code step width differences from the ideal converter characteristics, measured using the best-fit line.

- For the transfer function shown in the third previous slide, it shows how each code step width differs from ideal step width.
  
  - Assume each small X-axis division represents a sample.
  - The table shows the statistics for the first five codes of this converter. Each matrix \((T,D,C,E)\) is indexed by the output ADC code.
  - The ideal step width is 6, and the average actual is 6.8.
## Static Linear Histogram

DNL and INL in RMS LSB

<table>
<thead>
<tr>
<th>Code Count</th>
<th>$T (0)$</th>
<th>$T (1)$</th>
<th>$T (2)$</th>
<th>$T (3)$</th>
<th>$T (4)$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>3 + 3 = 6</td>
<td>5</td>
<td>4</td>
<td>11</td>
<td>8</td>
</tr>
<tr>
<td><strong>DLE (LSB fraction)</strong></td>
<td>$D (0)$</td>
<td>$D (1)$</td>
<td>$D (2)$</td>
<td>$D (3)$</td>
<td>$D (4)$</td>
</tr>
<tr>
<td></td>
<td>-0.1176</td>
<td>-0.2647</td>
<td>-0.4118</td>
<td>0.6176</td>
<td>0.1765</td>
</tr>
<tr>
<td><strong>DNL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.3650</td>
</tr>
<tr>
<td><strong>Transfer Characteris. (counts)</strong></td>
<td>$C (0)$</td>
<td>$C (1)$</td>
<td>$C (2)$</td>
<td>$C (3)$</td>
<td>$C (4)$</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>5.5</td>
<td>10</td>
<td>17.5</td>
<td>27</td>
</tr>
<tr>
<td><strong>ILE (LSB fraction)</strong></td>
<td>$E (0)$</td>
<td>$E (1)$</td>
<td>$E (2)$</td>
<td>$E (3)$</td>
<td>$E (4)$</td>
</tr>
<tr>
<td></td>
<td>0</td>
<td>-0.19115</td>
<td>-0.5294</td>
<td>-0.4265</td>
<td>-0.02945</td>
</tr>
<tr>
<td><strong>INL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.3161</td>
</tr>
</tbody>
</table>
Flash ADC Testing Method
Flash A/D Converter
Basic characteristics:

- Operates at 20 to 100 Mega samples per second, and even up to 250 Ms/s.
- They are code dominated converters.
  - Each step can have an error different from the other steps.
- There are no major carries in the converter, and so each code must be tested.
Static Linear Histogram Technique with a Triangular Wave

We use a very slow triangle wave.
- Ramps from just below the minimum full-scale voltage to a voltage just above the maximum full-scale voltage, and back down again.
- The ramp should be slow enough so that for each code, it will be digitized roughly 10 times before the ramp moves to the next code.

The ramp is repeated for up to 150 periods.
- To get the average behavior.

The code histogram is shown on next slide.
Linear Histogram of 8-bit Flash ADC

8-BIT FLASH CONVERTER LINEAR HISTOGRAM

N = 2048
AVERAGE STEP WIDTH = 7.799 COUNTS

13 COUNTS

4 COUNTS
MISSING CODE 215

1 CODE NUMBER

254
To find DLE ....

- To find DLE, we subtract the average count from each tally, and express that in units of LSBs.
- The test waveform is repeated 100 to 150 times.
- The DLE of an 8-bit ADC is shown on next slide.
  - This test can detect missing converter codes.
Example DLE Function

8-BIT ADC DIFFERENTIAL LINEARITY ERROR (DLE) HISTOGRAM OF 2048 COUNTS

DLE

Code

RMS DLE = 0.21 LSB - 1 LSB

+0.67 LSB
Integral Linearity Error (ILE)

\[ ILE[i] = ILE[i-1] + \frac{(DLE[i] + DLE[i-1])}{2} \]

ILE calculated from 4096-point histogram from previous ADC

Average = -0.52 LSB

RMS ILE = 0.59
STD DEV. = 0.27
RANGE = -1.19 TO +0.20
RANGE RELATIVE TO AVERAGE = -0.67 TO +0.72 LSB
DAC Testing Methods

- Problems with DAC testing:
  - A 16-bit DAC has a step size of 15 parts per million (ppm).
  - Requires a measurement accuracy of 2 ppm.

- Problems with direct measurement of DAC transfer map:
  - A 16-bit DAC has 65536 codes; 24-bit has 16777216. Takes too long to look at all of these.
    - We need to look at a subset.
  - A direct measurement demands very high accuracy, since we restrict measurement error to ±0.1 LSB.
The implication:

- A direct measurement of DAC transfer map is inappropriate.
- We can measure each interval in the transfer map, but we cannot measure each step directly, because the voltages defining it happen at different time instants.
Differential Measurement

\[ V_x : \text{smaller adjacent voltage} \]
\[ V_y : \text{larger adjacent voltage} \]
\[ C : \text{repeatable measurement error} \]
\[ e : \text{non-repeatable peak measurement error} \]

- We want to find

\[ (V_y + C + e) - (V_x + C + e) = V_y - V_x \pm 2e \]
- For 14 bits, the step size becomes 61 ppm (610 \( \mu \text{V} \) in a 10 V range DAC).
- We limit 2e to 61 \( \mu \text{V} \) to keep measurement error to 6.1 ppm, so e is only 30.5 \( \mu \text{V} \) \( \Rightarrow \) too hard and expensive
D/A Differential Test Fixture

- We measure the \((V_y - V_x)\) difference, not the absolute \(V_x\) or \(V_y\).
  - By comparing the difference to a biased, programmable supply \(V_b\)
  - \(V_b\) need not be accurate; just stable.
  - We measure \((V_x - V_b)\) and \((V_y - V_b)\)
Derivation of INL Measure

- Proposed by Mahoney et al [1981]
Summary

- DSP-based tester has:
  - Waveform Generator
  - Waveform Digitizer
  - High frequency clock with dividers for synchronization

- A/D and D/A Test Parameters
  - Transmission
  - Intrinsic

- A/D and D/A Faults: offset, gain, non-linearity errors
  - Measured by DLE, ILE, etc.

- A/D Test Histograms – static linear and sinusoidal
- D/A Test — Differential Test Fixture