Logic BIST Architecture
Motivation

• Complex systems with multiple chips demand elaborate logic BIST architectures
  – BILBO and test / clock system
    • Shorter test length, more BIST hardware
  – STUMPS & test / scan systems
    • Longer test length, less BIST hardware
  – Circular Self-Test Path
    • Lowest hardware, lower fault coverage

• Benefits: cheaper system test, Cost: more hardware.

• Must modify fully synthesized circuit for BIST to boost fault coverage
  – Initialization, loop-back, test point hardware
Built-in Logic Block Observer (BILBO)

- Combined functionality of D flip-flop, *pattern generator*, *response compacter*, & *scan chain*
  - Reset all FFs to 0 by scanning in zeros
Example BILBO Usage

- **SI** – Scan In
- **SO** – Scan Out
- **Characteristic polynomial**: $1 + x + \ldots + x^n$
- CUTs A and C: BILBO1 is MISR, BILBO2 is LFSR
- CUT B: BILBO1 is LFSR, BILBO2 is MISR

(a) Example test configuration.
BILBO Serial Scan Mode

• $B1 \text{ } B2 = "00"

• Dark lines show enabled data paths
BILBO LFSR Pattern Generator Mode

- $B_1 B_2 = \text{"01"}$
BILBO in D FF (Normal) Mode

- $B1 \ B2 = \text{“10”}$
BILBO in MISR Mode

- $B_1 B_2 = \text{“11”}$
Test / Clock System Example

- New fault set tested every clock period
- Shortest possible pattern length
  - 10 million BIST vectors, 200 MHz test / clock
  - \( \text{Test Time} = \frac{10,000,000}{200 \times 10^6} = 0.05 \text{ s} \)
  - Shorter fault simulation time than test / scan
Test / Scan System

- New fault tested during 1 clock vector with a complete scan chain shift
- Significantly more time required per test than test / clock
  - **Advantage**: Judicious combination of scan chains and MISR reduces MISR bit width
  - **Disadvantage**: Much longer test pattern set length, causes fault simulation problems
- Input patterns – time shifted & repeated
  - Become correlated – reduces fault detection effectiveness
  - Use XOR network to phase shift & decorrelate
STUMPS Example

- $SR_1$ ... $SR_n$ – 25 full-scan chains, each 200 bits
- 500 chip outputs, need 25 bit MISR (not 5000 bits)
STUMPS

- **Test procedure:**
  1. Scan in patterns from LFSR into all scan chains (200 clocks)
  2. Switch to normal functional mode and clock 1 x with system clock
  3. Scan out chains into MISR (200 clocks) where test results are compacted
     - Overlap Steps 1 & 3

- **Requirements:**
  - Every system input is driven by a scan chain
  - Every system output is caught in a scan chain or drives another chip being sampled
Alternative Test / Scan Systems

(a) Simple system.

(b) Alternative system.
Summary

• Logic BIST system architecture:
  – **Advantages:**
    • Higher fault coverage
    • At-speed test
    • Less system test, field test & diagnosis cost
  – **Disadvantage:** Higher hardware cost

• Architectures: BILBO, test / clock, test / scan

• Needs DFT for initialization, loop-back, and test points.